-- Figure 5B is a logical block diagram illustrating another scan chain segment 515 on which the present invention can be applied. As illustrated, the scan chain segment 515 includes scan cells 520p-520t which consist of multiplexed D input flip-flops linked together to form a shift register configuration. Also illustrated is clock buffer 526 which is inserted on the clock signal line 531 between cells 520s and 520t. --

2. Please replace the second paragraph on page 26 beginning with "It is also desirable..." has been replaced with the following paragraph:

-- It is also desirable to place simultaneously switching cells on different power rails because the maximum amount of switching that happens in a design is typically during scan. Such requirements could limit the size of the partitions identified for re-ordering. Accordingly, at step 660, subsets 655 are individually partitioned according to simultaneously switching output (SSO) requirements of scan cells of the pertinent set. As illustrated, one subset 655b is partitioned into final sets 665a-665n at step 660. Data representative of the final sets 665a-665n is then provided to layout process 350 as partitioning information of the scan chain 605. --

3. The second paragraph on page 27 beginning with "It should be appreciated that..." has been replaced with the following paragraph:

-- It should be appreciated that the order in which steps 610, 620, 630, 640, 650, and 660 of Figure 6 are performed is immaterial. Rather, the aforementioned steps may be performed in an arbitrary order. For instance, scan chain partitioning step 660 based on SSO requirements may be performed prior to partitioning step 650. Furthermore, one